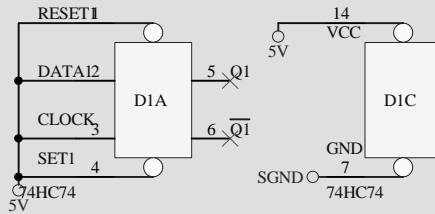
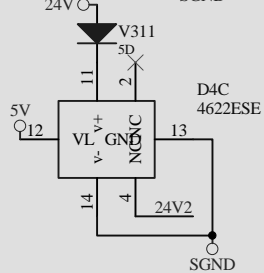
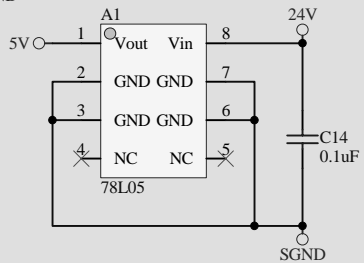
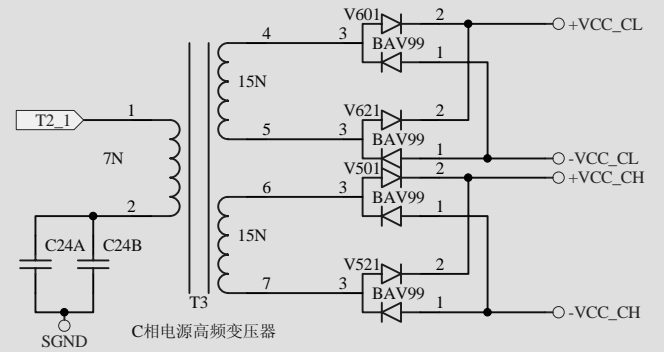
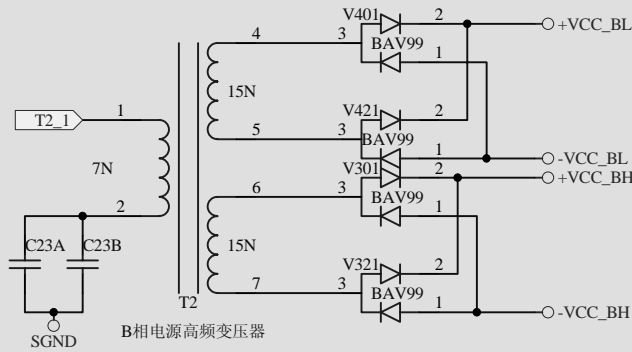
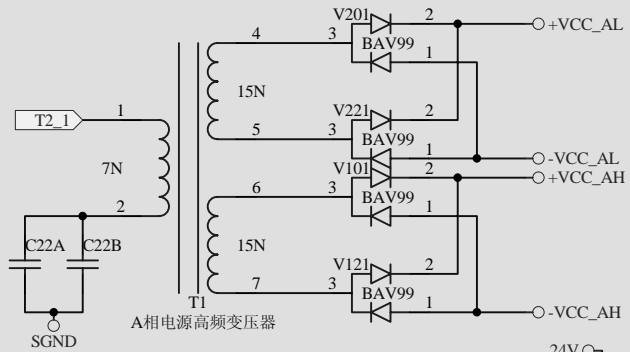
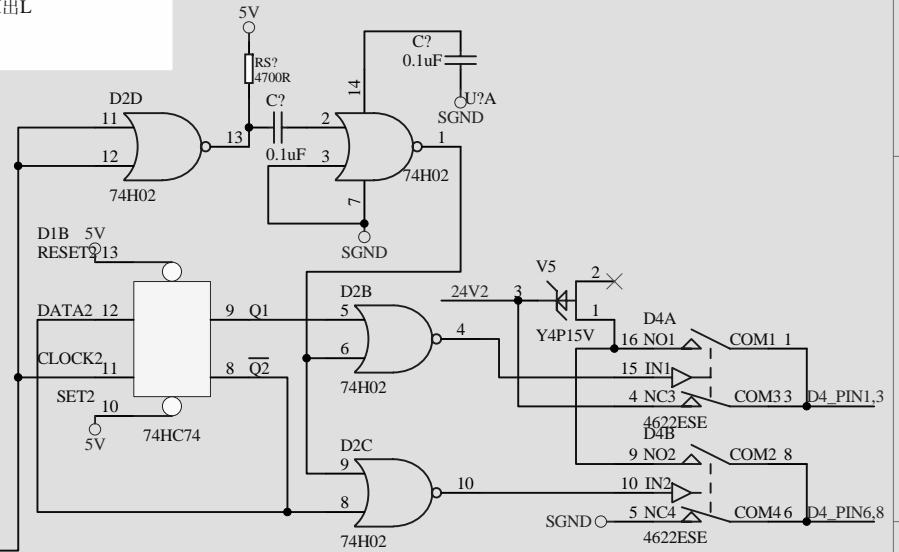
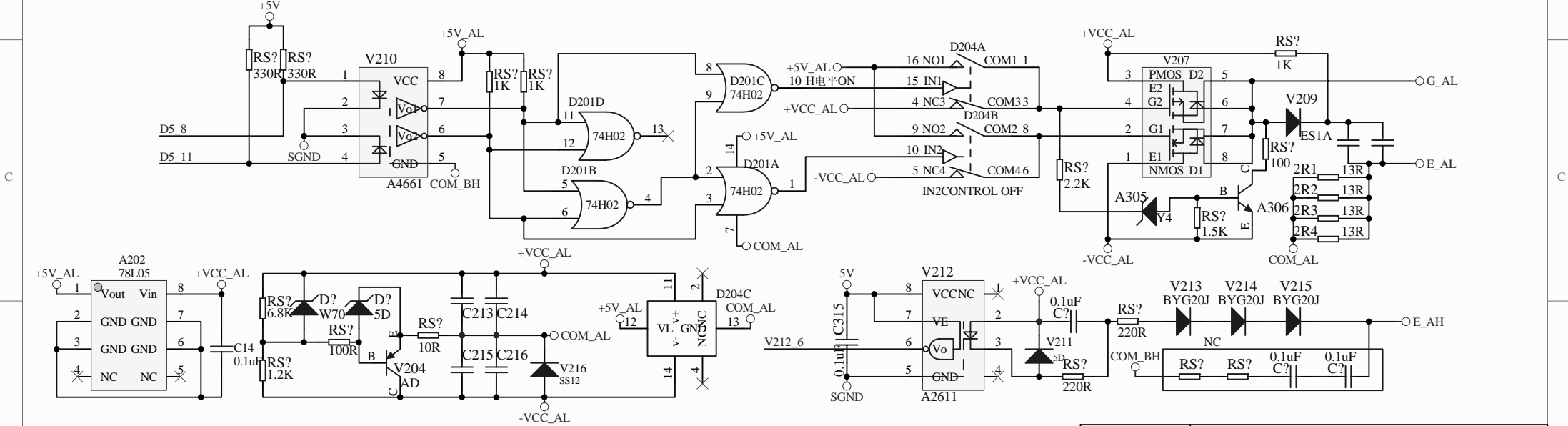
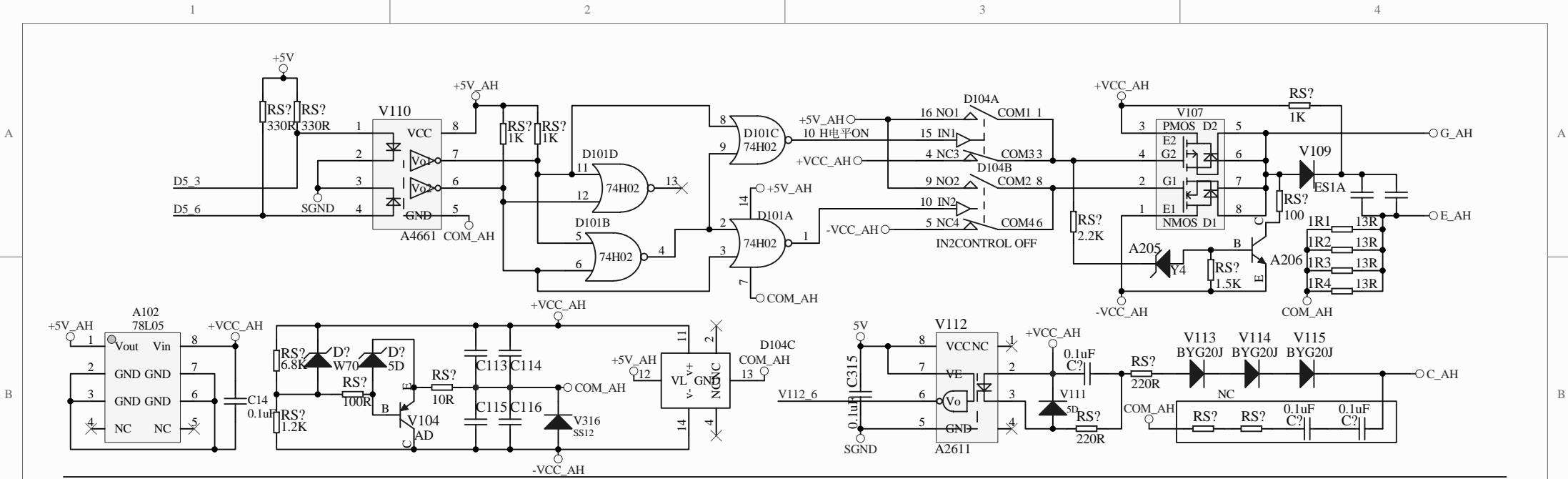


74HC02
:四个二输入或非门,有L出L,
全L出H全H出L



IPER				
上海艾帕电力电子有限公司				
图纸名称: AGDR-71C DRIVE_AUXPOWER.SCH				
项目	制图	页码	图纸大小	A4
版本	审核	日期	文件编号	PEE-30-A



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版本	审核	日期	文件编号	PEE-30-A	

MAX4622ESE为逻辑开关，输入为低电平时刻，1，2SW OFF，34SW ON。输入为高电平时刻，1，2SW ON，34SW OFF。

A

B

C

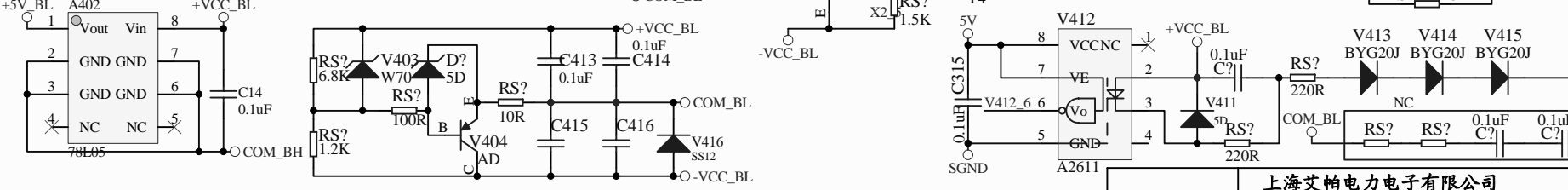
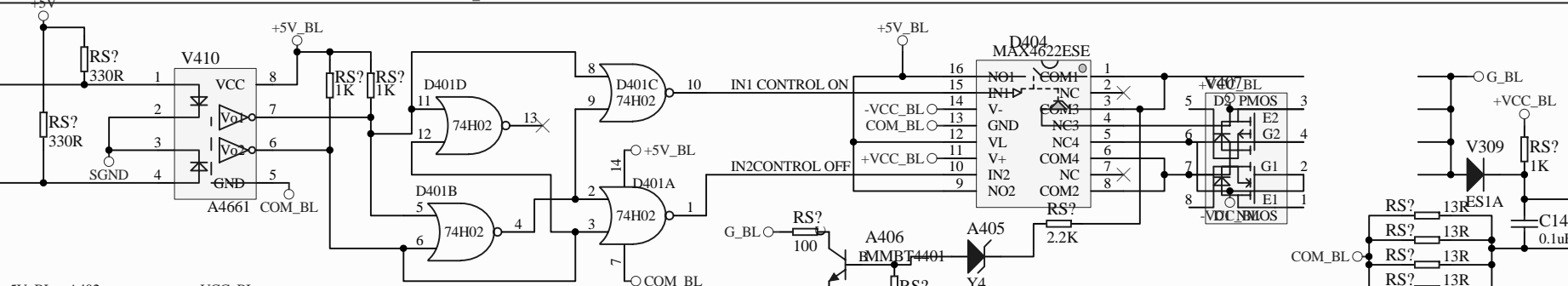
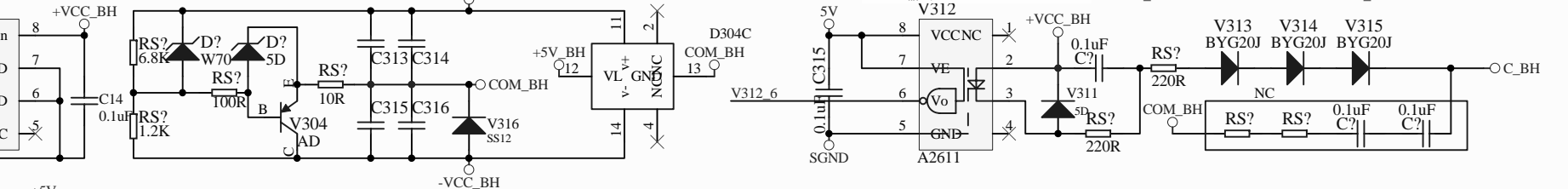
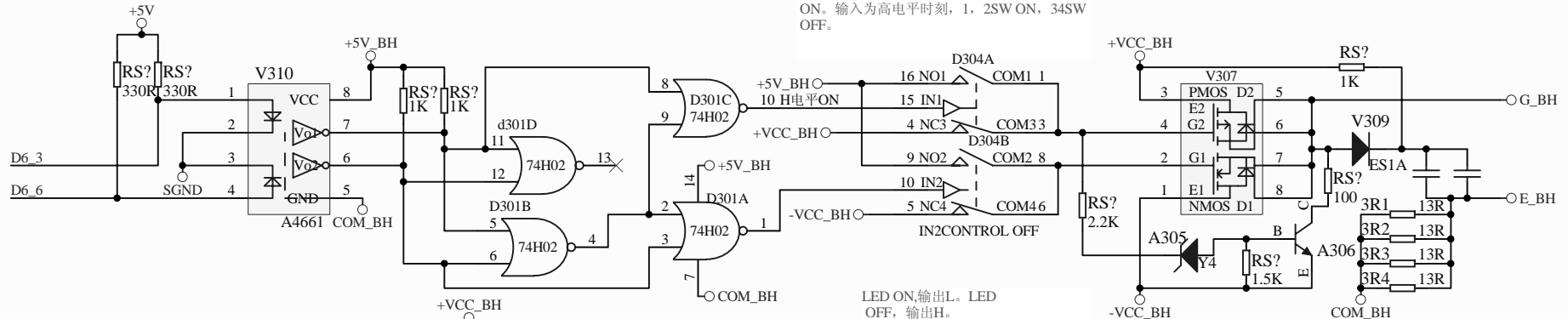
D

A

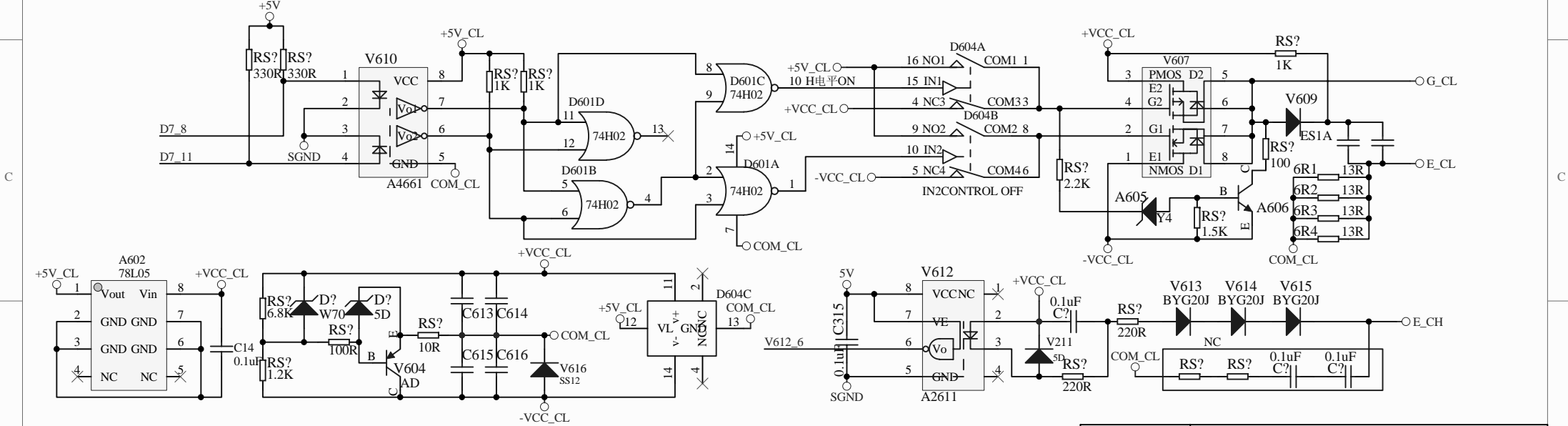
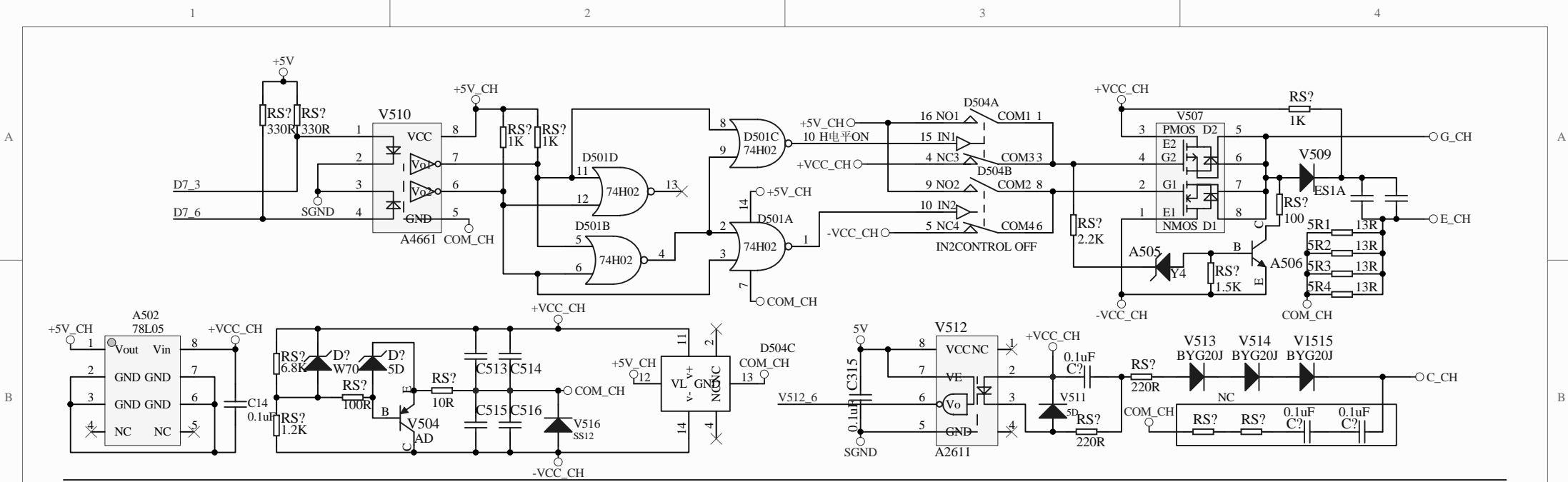
B

C

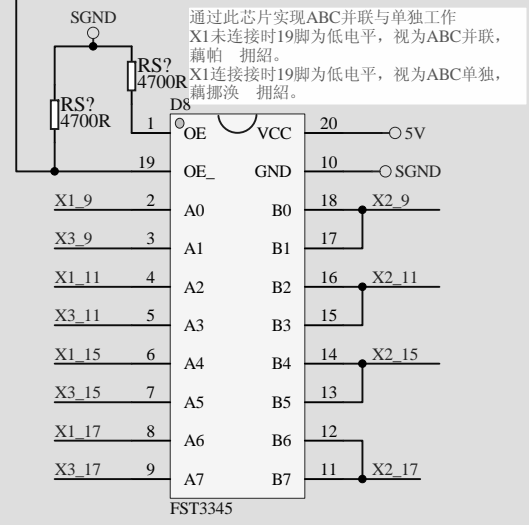
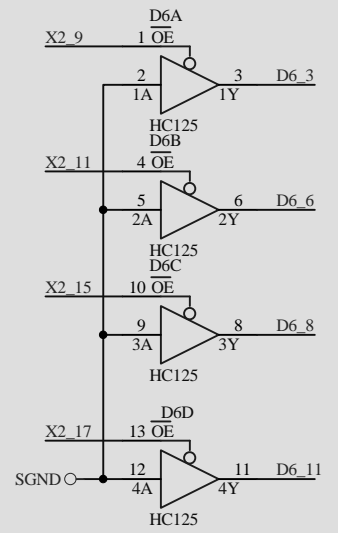
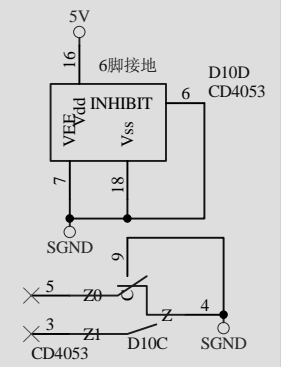
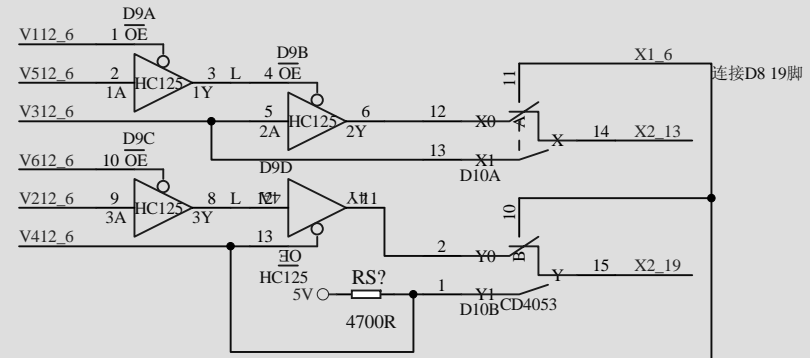
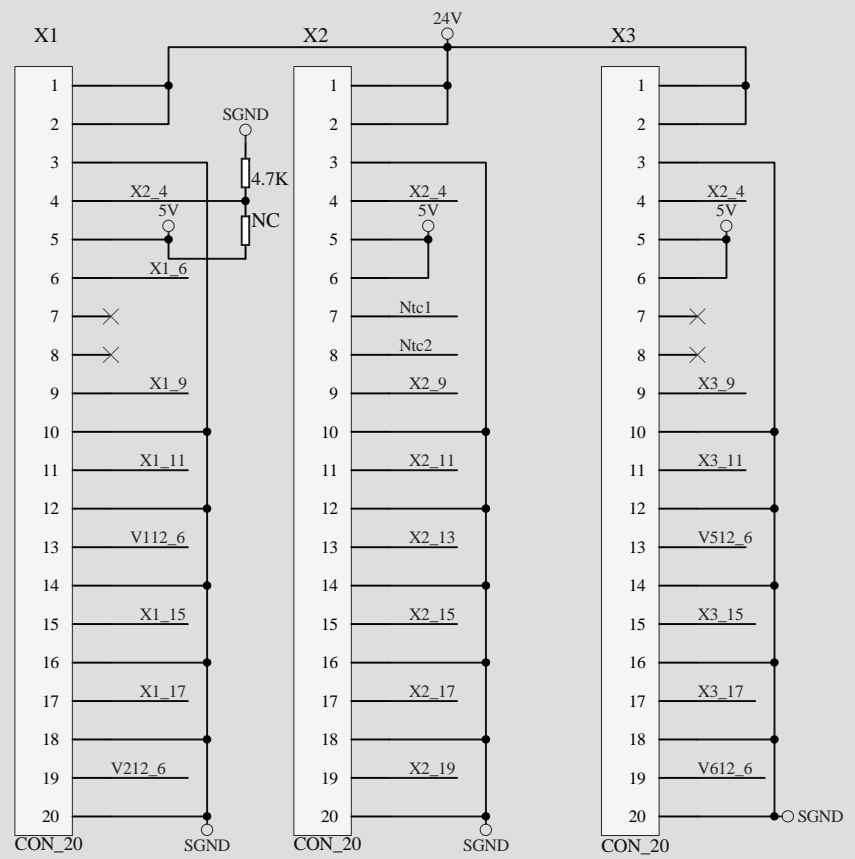
D



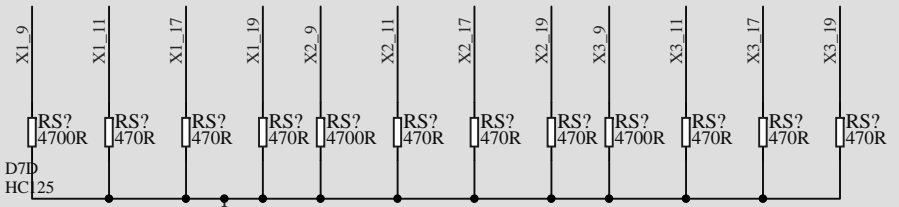
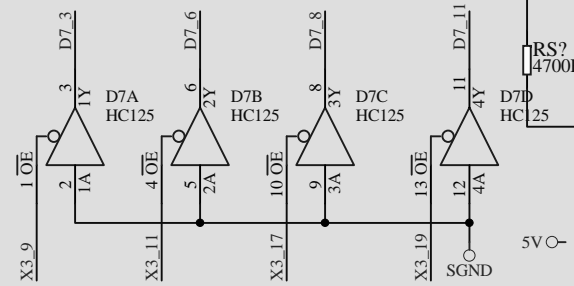
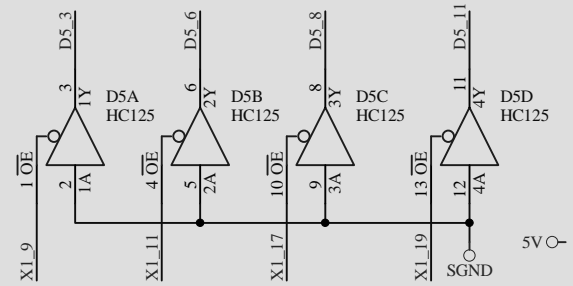
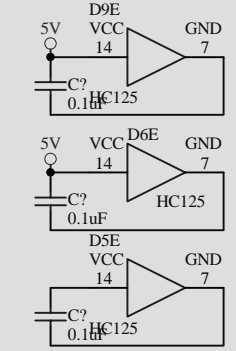
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		图纸名称: AGDR-71C DRIVE_PAHSE_B.SCH			
项目	制图	页码	图纸大小	A4	
版本	审核	日期	文件编号	PEE-30-A	



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版本	审核	日期	文件编号	PEE-30-A	



通过此芯片实现ABC并联与单独工作
X1未连接时19脚为低电平，视为ABC并联，
藕帕 捆绍。
X1连接时19脚为低电平，视为ABC单独，
藕挪浹 捆绍。



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		图纸名称: AGDR-71C DRIVE_IO.SCH			
项目	制图	页码	图纸大小	A4	
版本	审核	日期	文件编号	PEE-30-A	